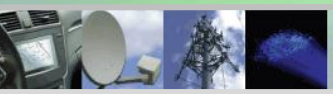

Hardware Users Guide

High Speed, Low Power
Analog-to-Digital Converter Evaluation Kits

EKIT01-HMCAD1510
EKIT01-HMCAD1511
EKIT01-HMCAD1520

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140-00036-00
CP110709 rev A

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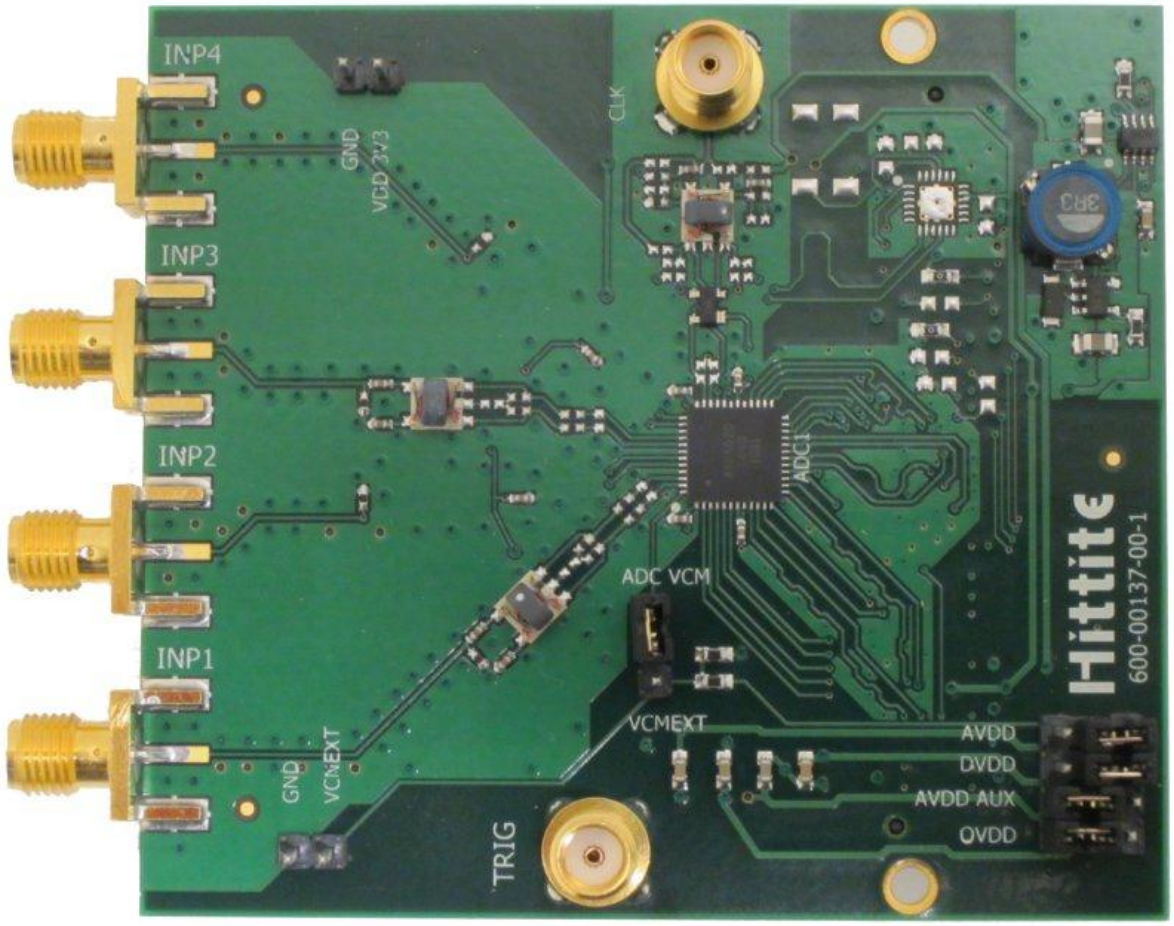
1 EVAL01-HMCAD15XX Hittite EasyBoard™



2 Introduction

This hardware user guide describes the physical components of the EVAL01-HMCAD15XX variants of EasyBoard™. These boards are a part of the EKIT01-HMCAD1510/1511/1520 evaluation kits. The kits consist of a Hittite EasyBoard™ FMC (FPGA Mezzanine Card) daughter board, a Xilinx FMC SP601 development mother board and the EasySuite™ software tool.

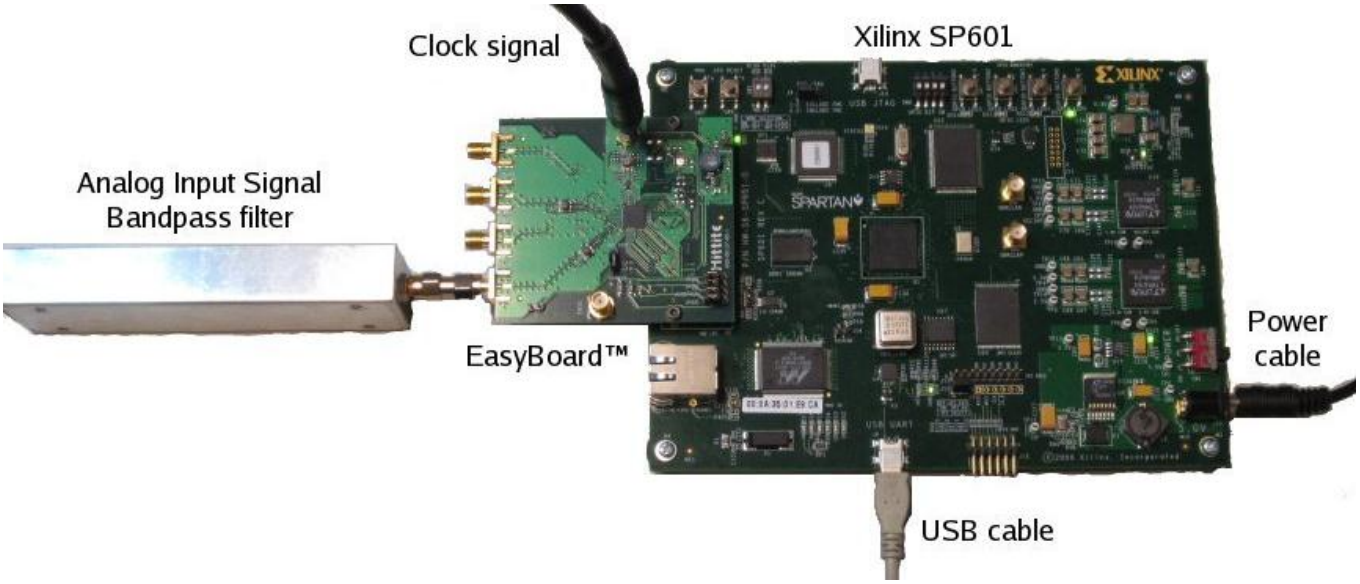
The EasyStack™ firmware is loaded on the Xilinx development board, which enables the configuration of the ADC and capture of data from the ADC.

The EKIT01-HMCAD15XX features Power Monitoring and Supply Voltage Adjustment.

3 Installation of Evaluation Kit

To use the Evaluation Kit, the following components are required:

- EVAL01-HMCAD1510, 1511 or 1520 EasyBoard™ (included in the kit)
- SP-601, Xilinx development board with EasyStack™ (included in the kit)
- Clock source
- Signal source
- PC with EasySuite™ software tool installed (software included in the kit)



Refer to Software Users Guide for EasySuite™ for installation of the EasySuite software.

4 Analog Inputs

4.1 Signal Quality

The quality of the input signal is the most important criterion to obtain good measurement results. The following points must be taken into consideration.

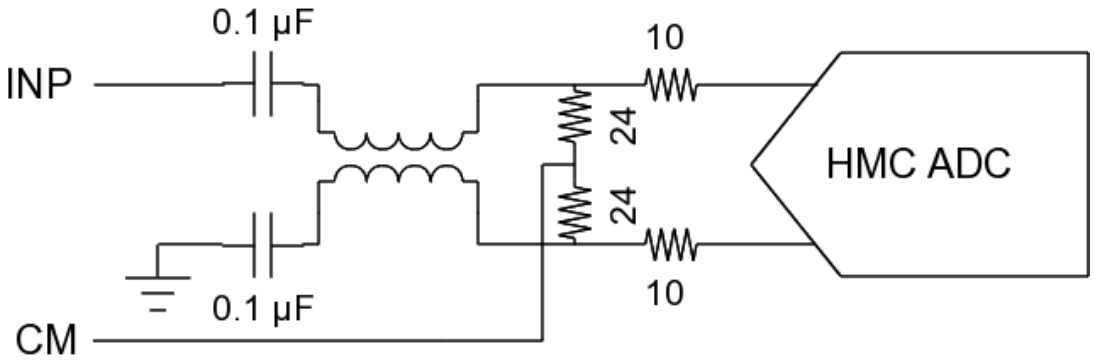
Select a signal source with low noise and low phase noise. Excellent results are obtained with the Agilent E8663.

Apply a bandpass filter between the signal source and the EasyBoard™ RF input (INP1 thru INP4). This is required to obtain sufficiently low white noise levels and to reduce harmonic components from the signal source. Excellent results have been obtained with the TTE (www.tte.com) filter series Q56T or KC4T. Make sure that large magnetic cores are used in the filters to avoid nonlinearity due to core saturation. Alternative vendors are K&L

Microwave (www.klmicrowave.com) and Allen Avionics Inc. (www.allenavionics.com). The input signal (after filtering) could be checked with a spectrum analyzer to ensure that noise and harmonic levels are significantly better than the theoretical contribution from the ADC.

4.2 Analog input network

The input network of the EasyBoard™ is configured with an AC coupled balun. This balun converts the single ended input to a differential input for the ADC.



4.3 Clock Generation

The clock inputs on the HMCAD15XX ADCs accept CMOS, LVDS, LVPECL and sine wave inputs. Connect a clock source to the SMA connector named CLK. The EasyBoard™ clock network is an AC coupled balun configuration with a 20MHz lower frequency limit. The network will accept a single ended sine wave or square wave input.

For best possible performance it is very important that the clock source have low jitter. Poor jitter performance will directly result in reduced SNR. The SNR contribution from jitter is given by equation (1) assuming a full scale input signal at frequency, FIN, and TRMS-jitter, measured in second Root-Mean-Square.

$$SNR = -20 \times log(2\pi \times F_{IN} \times T_{RMS}) \quad (1)$$

One can see that a 1ps clock jitter with a 25 MHz full scale input signal results in an additional SNR component of 76 dBc. Because of this the clock signal should be treated with the same care as the analog inputs to the ADC.

It is possible to reconfigure the board to accept a clock generated directly from the FPGA or from a clock generator located on the Xilinx Spartan-6 evaluation board.

Contact adc@hittite.com for instructions on how to reconfigure the board.

4.4 TRIG input

This connector is directly routed to a general IO pin on the FPGA. It can be used to apply an external trigger.

5 Jumpers and connectors

5.1 Power domains

JP4/JP5 in lower right corner, see section 9.1, must be set to enable power for all power domains to the converter. There should be one jumper on each row, ether to the right or the left. Setting the jumper to the right, will include that power domain in the built in current measurement feature. Setting the jumper to the left, the current measurement for that domain will be bypassed.

All the power domains are on the 1.8 V power supply. They are separated on the board so that it is possible to measure the current consumption individually for each power domain on the chip. The domains are as follows:

- AVDD is the analog power domain and includes all power consumption in the ADC cores.
- DVDD is the digital power domain and includes power consumption in the digital block and the LVDS IO drivers.
- AVDD_AUX is the power domain for the reference circuit.
- OVDD is the domain for the IO ring on the pads inside the chip. In effect it only drives the configuration SPI signals.

5.2 Common mode

JP1, see section 9.1, selects the source for common mode drive. This is the common mode level for the differential input signals. If the jumper is placed in the top position, the common mode is driven by the ADC's common mode output. The drive strength of this output is programmable from the configuration software. See the datasheet for details around this drive strength.

If the jumper is placed in the lower position, the common mode is set by two on board 51 ohms resistors between the 1.8 V supply and ground. It is possible to override this common mode externally by connecting a voltage source to the terminal port JP2 in the lower left corner.

5.3 3.3 V supply output

Terminal JP5 offers a 3.3 V supply output. This supply originates from the power converters on the mother board, for instance SP601. It can drive a load up to around 5 A. This terminal can be used as a power supply for an external crystal oscillator, for instance RFPRO33-1000.000 from Crystek Corporation, which can be used as a clock source.

5.4 FMC connector

The FMC (FPGA Mezzanine Card) connector, J1, is located on the backside of the board. Connect this with the FMC connector on the Xilinx® mother board.

6 Special features

6.1 Power monitoring

U4 is a power monitoring chip. This can measure the current consumption and voltage level for the ADC. See 5.1 Power domains for details about measuring different power domains on the ADC. If all jumpers on JP4/JP5 are placed to the right, the total power consumption of the chip is measured.

The EasySuite™ software controls and collects data from the monitoring chip.

If the power measurement gives unexpected results, try to bypass the OVDD domain from the power measurement circuit.

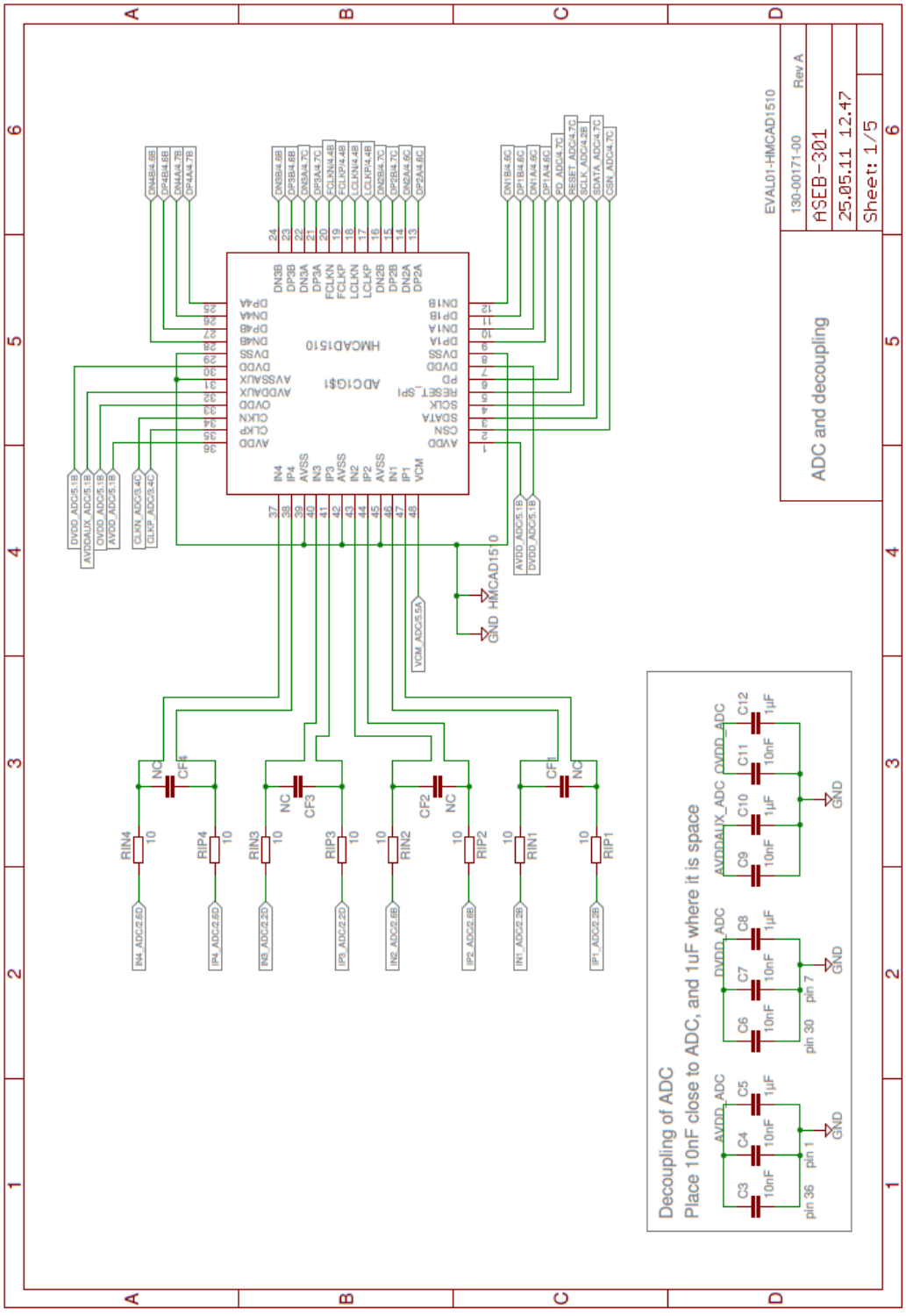
6.2 Supply voltage level

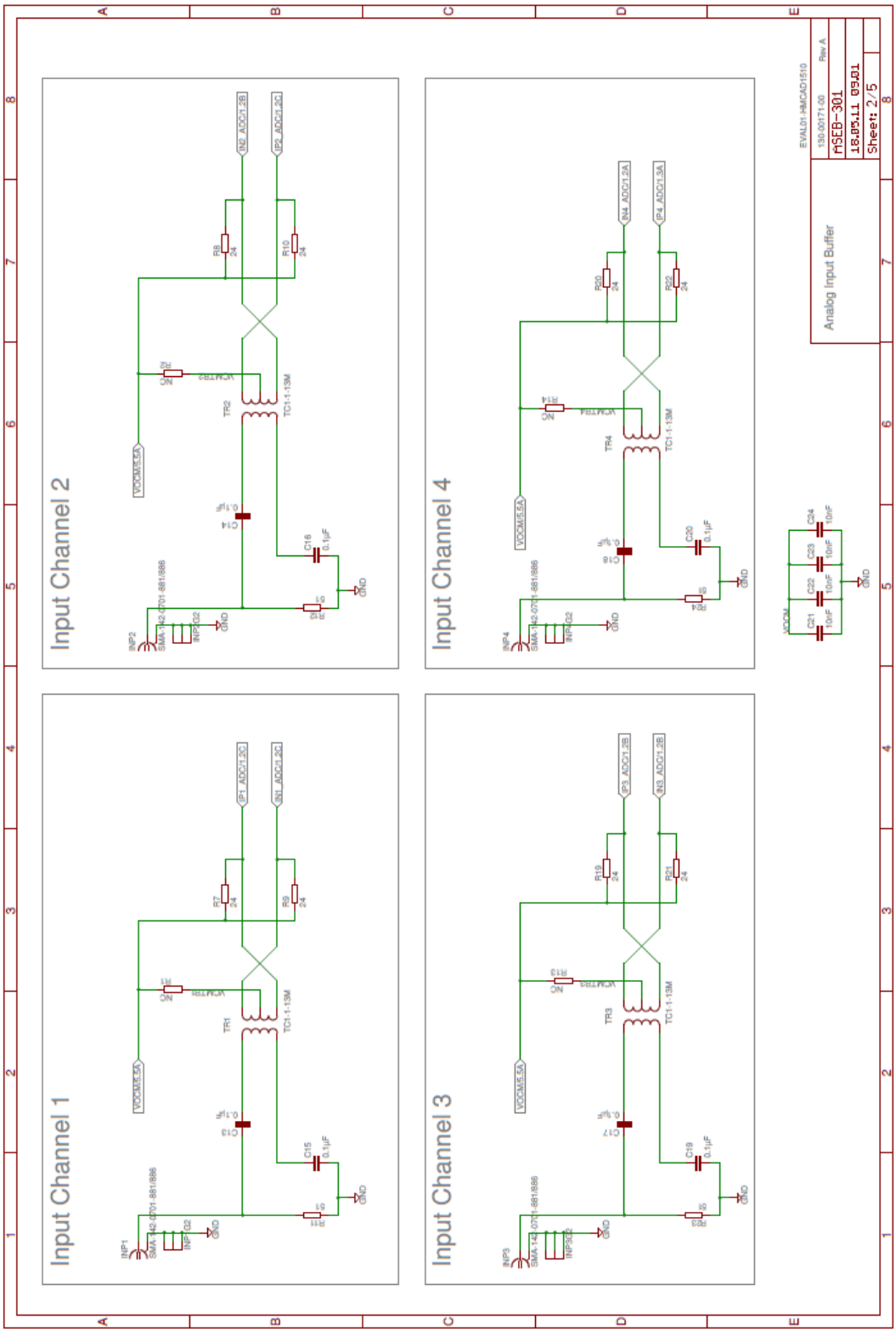
The supply voltage level for the ADC can be adjusted through the EasySuite™ software. U12 is a digital potentiometer which can adjust the supply level between 1.7 V and 2.0 V. Refer to the EasySuite™ Software User Guide for an explanation of how to set the supply voltage.

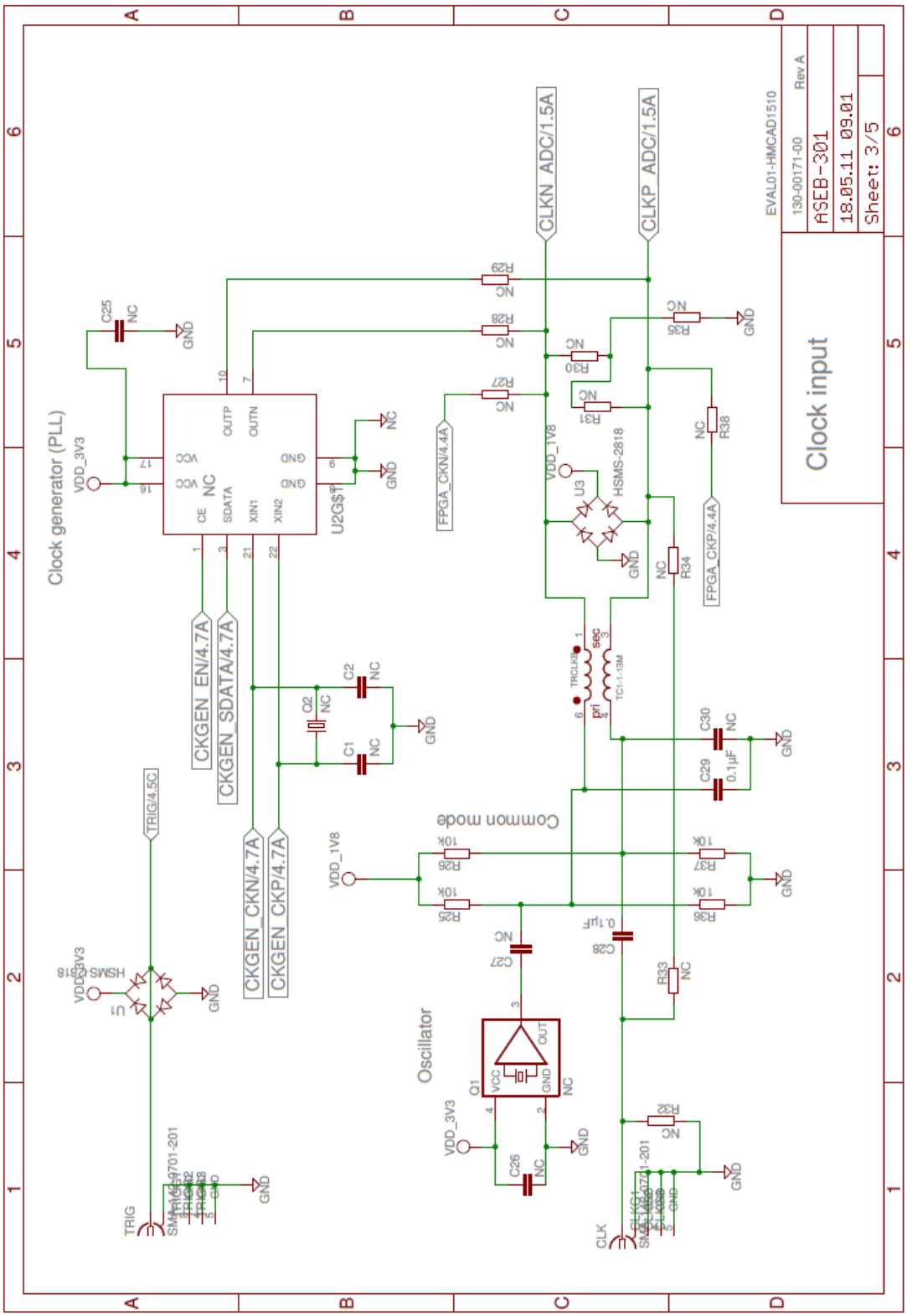
7 List of material

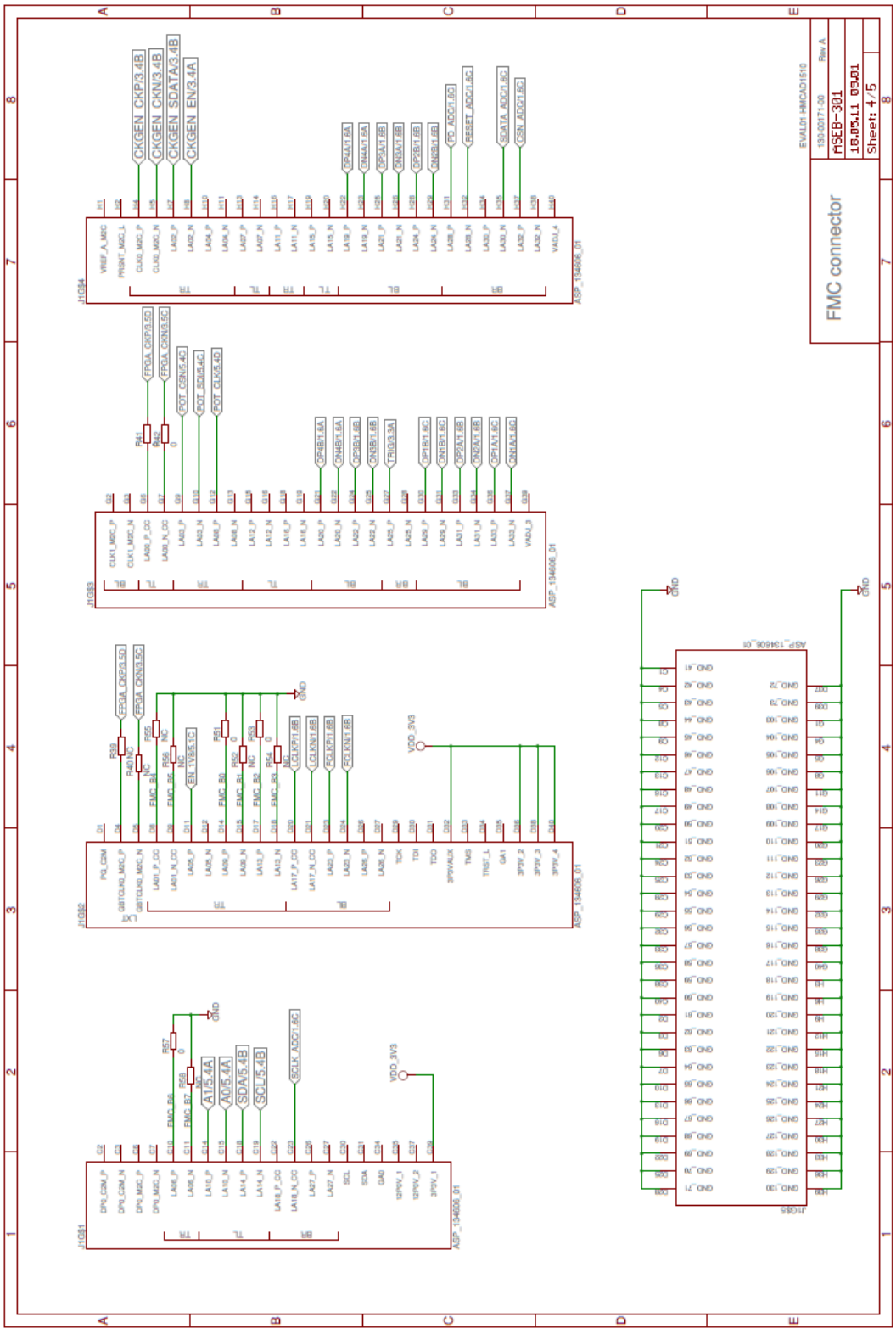
Qty	Refdes	Description
1	ADC1	HIGH SPEED MULTI-MODE 12/14-BIT 40 TO 640 MSPS A/D CONVERTER
1	D1	RECT SCHOTTKY 30V 1.5A 3-2A1A
1	J1	CONN SNGL-END ARRAY MALE 160POS
1	JP1	TERMINAL STRIP, SINGLE ROW 3 PIN .100", TRW
1	JP3	TERMINAL STRIP, SGL ROW 4 PIN TH .100", TLW
1	JP4	TERMINAL STRIP, DUAL ROW 2X4 TH .100", TLW
1	L13	INDUCTOR SHIELD PWR 3.3UH 7045
1	R45	RES 0.20 OHM 1/4W 1% 0805 SMD
1	R48	RES 100K OHM 1/10W 1% 0603 SMD
1	R50	RES 10.0K OHM 1/10W 1% 0603 SMD
1	U12	IC POT DGTL SPI 256POS SOT23-8
1	U4	IC CURRENT MONITOR 1% SOT23-8
1	U5	IC REGULATOR BUCK 1.5A SOT23-5
2	C34-C35	CAP CER 47UF 6.3V X5R 20% 0805
2	CLK,TRIG	CONN RECEPT STRAIGHT PCB .155" G
2	JP2,JP5	TERMINAL STRIP, SGL ROW 2 PIN TH .100", TLW
2	R3,R49	RES 20K OHM 1/10W 1% 0603 SMD
2	R41-R42	RES ZERO OHM 1/16W 5% 0402 SMD
2	R43-R44	RES 51 OHM 1/10W 1% 0603 SMD
2	U1,U3	Schottky Diode, RF, Bridge Quad
4	INP1-INP4	SCD, MA-F, EGDE LAUNCH, .031" BOARD, JOHNSON
4	R11-R12,R23-R24	RES 51 OHM 1/10W 1% 0402 SMD
4	R25-R26,R36-R37	RES 10.0K OHM 1/16W 1% 0402 SMD
5	R46-R47,R51,R53,R57	RES ZERO OHM 1/10W 5% 0603 SMD
5	TR1-TR4,TRCLKB	RF TRANSFORMER, 50 OHM, 4.5-3000MHz, TC1-1-13M+
8	C5,C8,C10,C12,C31-C33,C44	CAP CER 1UF 25V 15% X5R 0603
8	R7-R10,R19-R22	RES 24 OHM 1/10W 1% 0402 SMD
8	RIN1-RIN4,RIP1-RIP4	RES 10 OHM 1/10W 1% 0402 SMD
10	C13-C20,C28-C29	CAP CER .1UF 50V 10% X7R 0402
10	C3-C4,C6-C7,C9,C11,C21-C24	CAP CER .01UF 50V 10% X7R 0402
34	C1-C2,C25-C27,C30,CF1-CF4,Q1-Q2,R1-R2, R13-R14,R27-R35,R38-R40,R52,R54-R56, R58,U2	DO NOT POPULATE COMPONENTS

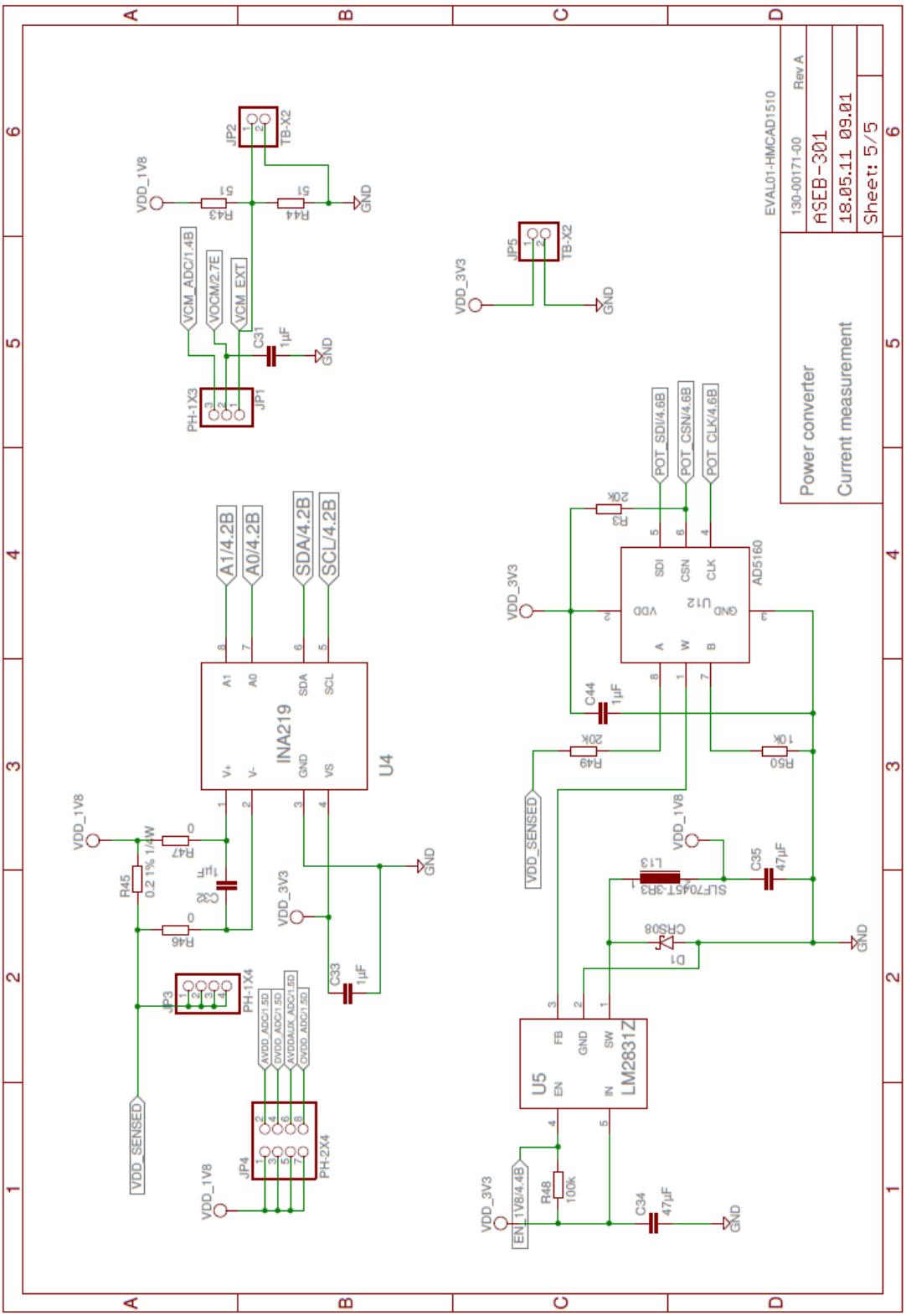
8 Schematics




Input Channel 2
Input Channel 4
Input Channel 1
Input Channel 3
Analog Input Buffer
EVAL01-HMCAD1510
Rev A
130-00171-00
rSEB-301
18.05.11 09:01
Sheet: 2/5

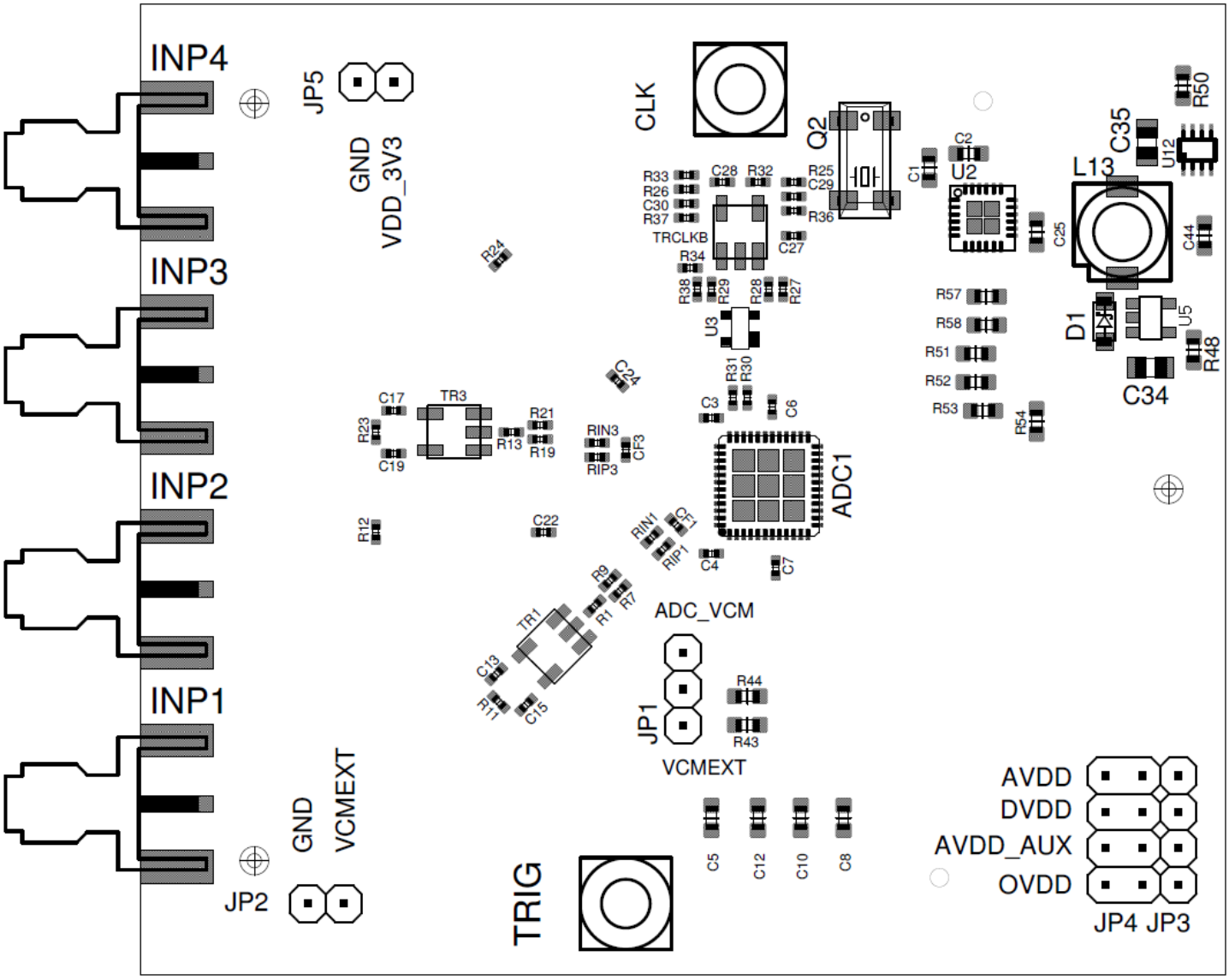

Clock input
EVAL01-HMCAD1510
Rev A
130-001171-00
ASEB-301
18.05.11 09.01
Sheet: 3/5
CLKN_ADC/1.5A
CLKP_ADC/1.5A
Clock generator (PLL)
VDD_3V3
CKGEN_EN/4.7A
CKGEN_SDATA/4.7A
CKGEN_CKN/4.7A
CKGEN_CKP/4.7A
FPGA_CKN/4.4A
FPGA_CKP/4.4A
Common mode
VDD_1V8
HSMS-2818
Oscillator
TRIG/4.5C
TRIG
CLK
GND
NC


FMC connector
CKGEN CKP/3.4B
CKGEN CKN/3.4B
CKGEN SDATA/3.4B
CKGEN EN/3.4A
FPGA_CKP/3.6C
FPGA_CKN/3.6C
POT_CSN/5.4C
POT_SDI/5.4C
POT_CLK/5.4C
A15/5.4A
A0/5.4A
SDA/5.4B
SCL/5.4B
SCLK_ADC/1.6C
GND
VDD_3V3

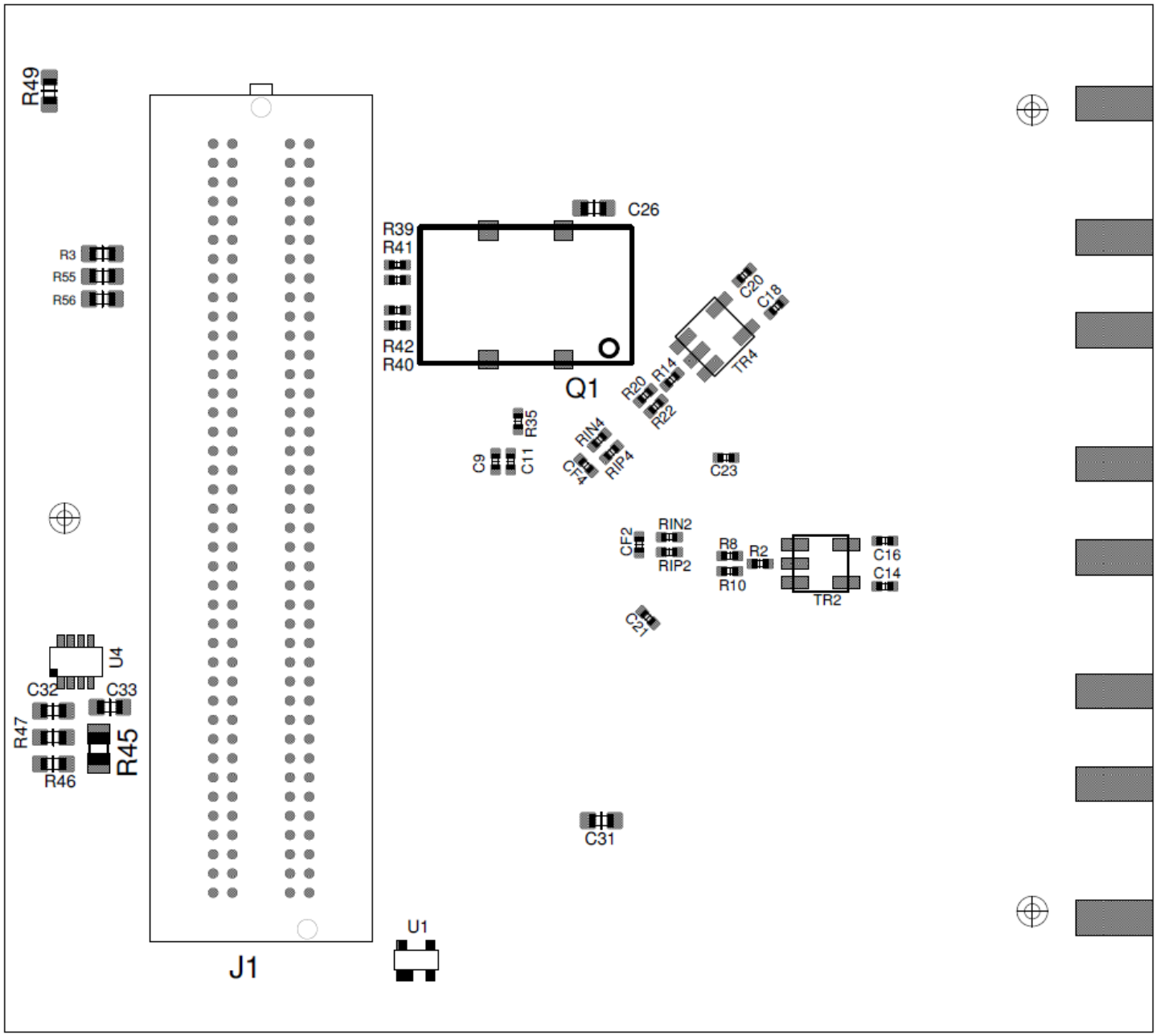

EVAL01-HMCAD1510
130-00171-00
Rev A
ASEB-301
18.05.11 09.01
Sheet: 5/5
Power converter
Current measurement
INA219
U4
AD5160
U12
LM28317
U5
JP1
JP2
JP3
JP4
JP5
TB-X2
PH-1X3
PH-1X4
PH-2X4
VDD_1V8
VDD_3V3
GND
VDD_SENSED
VCM_ADC/1.4B
VOCM/2.7E
VCM_EXT
A1/4.2B
A0/4.2B
SDA/4.2B
SCL/4.2B
POT_SDI/4.6B
POT_CSN/4.6B
POT_CLK/4.6B
EN_1V8/4.4B
AVDD_ADC/1.5D
DVDD_ADC/1.5D
AVDDAUX_ADC/1.5D
CVDD_ADC/1.5D

9 Physical layout

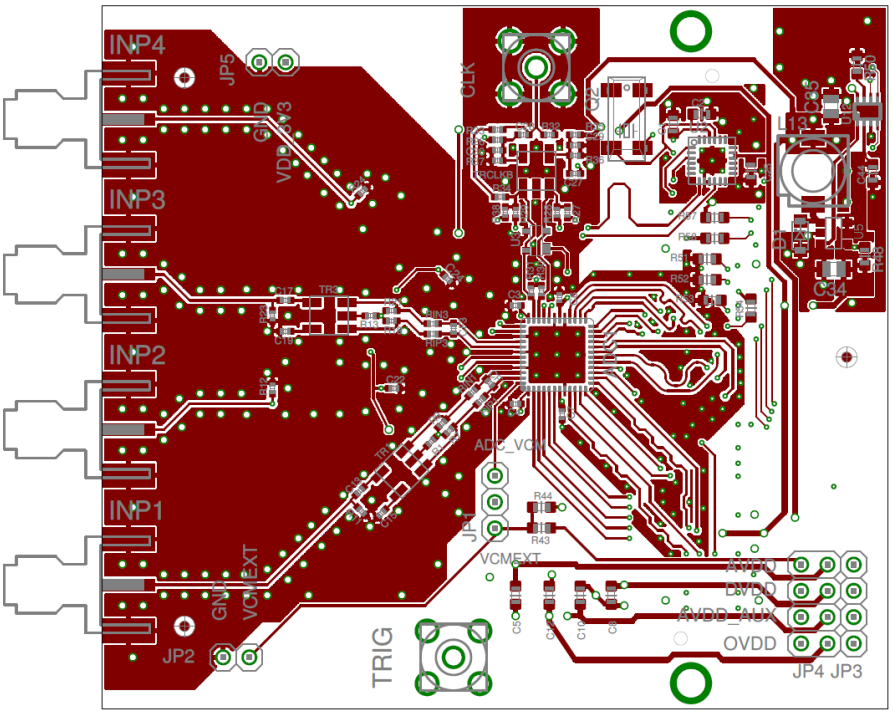
9.1 Component placement TOP



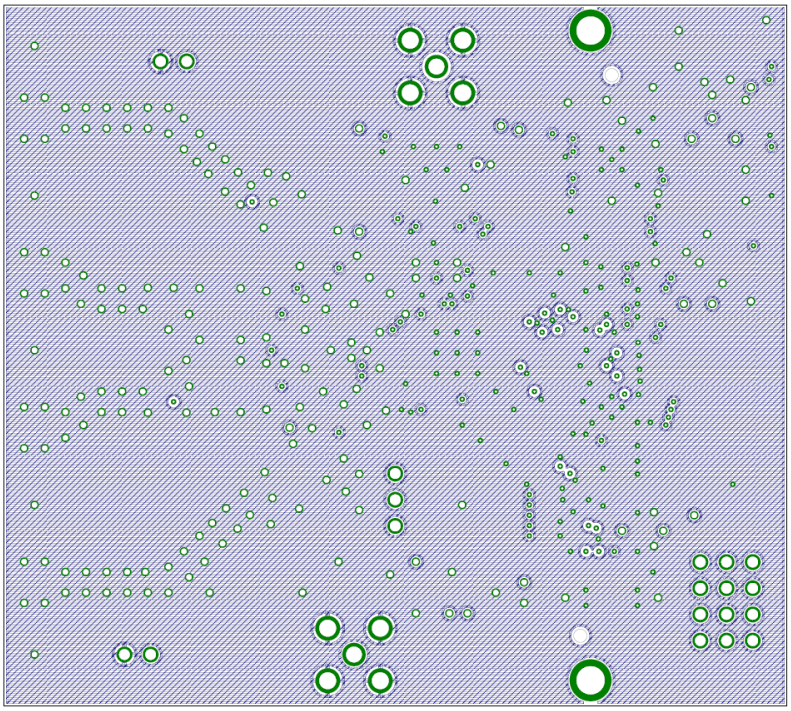
9.2 Component placement BOTTOM



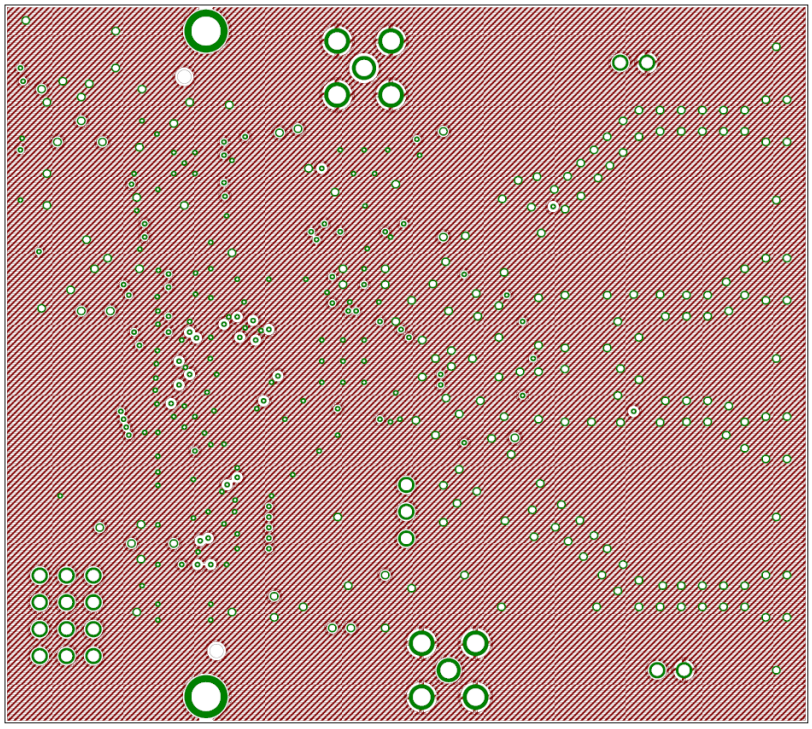
9.3 Top layer



9.4 Inner layer top



9.5 Inner layer bottom



9.6 Bottom layer